

CLAIMS

1. A frequency synthesizer, comprising:
 - 2 a digitally controlled oscillator, including a plurality of switched capacitors;
 - 4 control circuitry for selectively enabling and disabling said capacitors responsive to an oscillator tuning word, comprising:
 - 6 select circuitry for enabling a number of capacitors responsive to said oscillator tuning word;
 - 8 circuitry for dynamically varying which capacitors are enabled for a given oscillator tuning word to reduce non-linearities caused by slight
 - 10 variances in capacitive values.
2. The frequency synthesizer of claim 1 wherein said control circuitry
 - 2 further includes a switch matrix coupled to said select circuitry, said dynamically varying circuitry and said plurality of switched capacitors, said switch matrix
 - 4 having a plurality of switches selectively enabled by said select circuitry and said dynamically varying circuitry, said switches for enabling or disabling respective
 - 6 switched capacitors.
3. The frequency synthesizer of claim 2 and further comprising
 - 2 drivers coupled between said switches and respective capacitors.
4. The frequency synthesizer of claim 3 wherein said drivers comprise
 - 2 resampling drivers.
5. The frequency synthesizer of claim 2 wherein said switches are
 - 2 arranged in a plurality of predefined groups.
6. The frequency synthesizer of claim 5 wherein said dynamically
 - 2 varying circuitry varies a set of switches enabled in a group.

7. The frequency synthesizer of claim 6 wherein said dynamically
2 varying circuitry rotates said set of switches within a group.

8. The frequency synthesizer of claim 5 wherein said dynamically
2 varying circuitry varies a set of switches enabled in a plurality of groups.

9. The frequency synthesizer of claim 8 wherein said dynamically
2 varying circuitry rotates said set of switches within a plurality of groups.

10. A method of synthesizing a frequency, comprising the steps of:
2 selectively enabling and disabling capacitors in a digitally controlled
oscillator responsive to an oscillator tuning word; and
4 circuitry for dynamically varying which capacitors are enabled for a given
error signal value to reduce non-linearities caused by slight variances in
6 capacitive values.

11. The method of claim 10 wherein said selectively enabling step
2 comprises the step of selectively enabling and disabling switches in a switch
matrix responsive to said oscillator tuning word and said dynamically varying
4 step comprises the step of dynamically varying which switches are enabled for a
given error signal value.

12. The method of claim 11 wherein said switches are arranged in a
2 plurality of groups.

13. The method of claim 12 wherein said dynamically varying step
2 comprises the step of dynamically varying a set of switches enabled in a group.

14. The method of claim 13 wherein said dynamically varying step
2 comprises the step of rotating said set of switches within a group.

15. The method of claim 12 wherein said dynamically varying step
2 varies a set of switches enabled in a plurality of groups.

16. The method of claim 15 wherein said dynamically varying step
2 rotates said set of switches within said plurality of groups.

17. A frequency synthesizer comprising:
2 a digitally controlled oscillator, including a plurality of switched
capacitors; and
4 control circuitry for selectively enabling and disabling said capacitors,
comprising:
6 circuitry for tuning said digitally controlled oscillator to a selected
frequency by enabling and disabling capacitors in a first set; and
8 circuitry for modulating said digitally controlled oscillator by
enabling and disabling capacitors in a second set.

18. The frequency synthesizer of claim 17 wherein said tuning circuitry
2 comprises circuitry for initially enabling and disabling said capacitors in said
first set responsive to a oscillator tuning word while leaving said second set of
4 capacitors in a predetermined state.

19. The frequency synthesizer of claim 17 wherein said tuning circuitry
2 comprises circuitry for enabling and disabling said capacitors in said first set and
said second set responsive to a oscillator tuning word and, after obtaining said
4 selected frequency, rearranging the enabled and disabled capacitors such that the
second set of capacitors is in a predetermined state.

20. A method of synthesizing a frequency, comprising the steps of:
2 tuning a digitally controlled oscillator by enabling and disabling a first set
of switched capacitors to reach a selected frequency; and

4 modulating said digitally controlled oscillator by enabling and disabling a
second set of switched capacitors.

6 21. The method of claim 20 wherein said tuning step comprises the
step of initially enabling and disabling said capacitors in said first set responsive
8 to a oscillator tuning word while leaving said second set of capacitors in a
predetermined state.

22. The method of claim 20 wherein said tuning step comprises the
2 step of enabling and disabling said capacitors in said first set and said second set
responsive to a oscillator tuning word and, after obtaining said selected
4 frequency, rearranging the enabled and disabled capacitors such that the second
set of capacitors is in a predetermined state.

23. A frequency synthesizer comprising:

2 a digitally controlled oscillator, including a first set of switched capacitors
and a second set of switched capacitors, where said second set of switched
4 capacitors are in a physically separate area from said first set of switched
capacitors;

6 control circuitry for selectively enabling and disabling said capacitors
responsive to an oscillator tuning word, comprising:

8 first tracking circuitry for enabling and disabling capacitors
responsive to an first portion of said oscillator tuning word and a first clock;

10 second tracking circuitry for enabling and disabling capacitors
responsive to a second portion of said oscillator tuning word and a second clock,
12 wherein said second clock is significantly faster than said first clock.

24. The frequency synthesizer of claim 23, wherein said second
2 tracking circuitry includes a digital dithering circuit.

25. The frequency synthesizer of claim 24, wherein said digital
2 dithering circuit comprises a sigma-delta modulation circuit.

26. The frequency synthesizer of claim 23, wherein said first tracking
2 circuitry enables and disables capacitors in said first set responsive to an integer
portion of said oscillator tuning word and said second tracking circuitry enables
4 and disables capacitors in said second set responsive to a fractional portion of
said oscillator tuning word.

27. A method of synthesizing a frequency comprising the steps of:
2 enabling and disabling a first set of switched capacitors in a
digitally controlled oscillator responsive to a first portion of an oscillator tuning
4 word and a first clock;
enabling and disabling a second set of switched capacitors,
6 physically separate from said first set, in the digitally controlled oscillator
responsive to a second portion of an oscillator tuning word and a second clock,
8 wherein said second clock is significantly faster than said first clock.

28. The method of claim 27, wherein said step of enabling and
2 disabling said second set of capacitors comprises the step of modulating said
second set with a digital dithering circuit.

29. The method of claim 28 wherein said modulating step comprises
2 the step of modulating the second set using sigma-delta modulation.

30. The method of claim 27, wherein said step of enabling and
2 disabling said first set of capacitors comprises the step of enabling and disabling
said first set of capacitors responsive to an integer portion of said oscillator
4 tuning word and said step of enabling and disabling said second set of capacitors
comprises the step of enabling and disabling said second set of capacitors
6 responsive to a fractional portion of said oscillator tuning word.